SPLITTER_TRIGGER board - Board which split a bus of 32 differential ECL input into 3 bus of 32 differential ECL output and generate a conditional trigger signal in NIM mechanical module

J. Bouvier

Internal report LPSC 05-90
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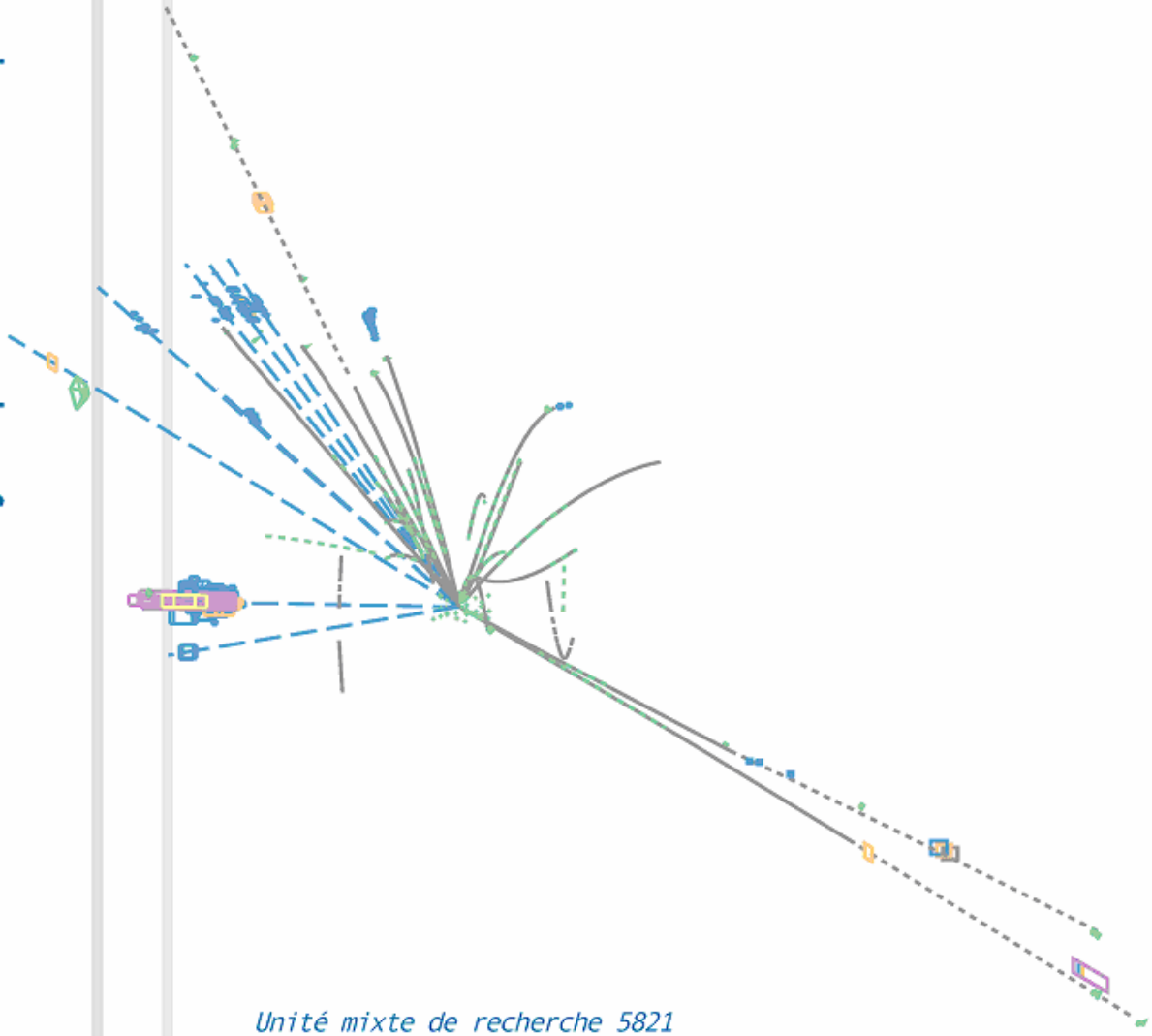
SPLITTER_TRIGGER board

Board which split a bus of 32 differential ECL input into 3 bus of 32 differential ECL output and generate a conditional trigger signal in NIM mechanical module.

Joel BOUVIER
Data Acquisition Team



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1. Overview

The purpose of this board is to generate a trigger signal, issued of 2 group of 16 input signals, for the CEDFPD board and to replicate three time this 2 group of 16 bit signal.

2. Input / output

IN A, IN B — this is 2 group of 16 input signals. Each signal is in complementary ECL technology (NECL). Each group are located on different connector (HE10 type connector). The pinout of the different connector are given in annex 10.
All the signal of a group must be driven due to the input signal technology. This technology of signals does not regard the signals off-line as being at the low state.

OUTPUT A1
OUTPUT A2
OUTPUT A3
OUTPUT B1
OUTPUT B2
OUTPUT B3

This is the replicated signals of the INA, INB input group signals delayed by a time defined inside the board by switch.
The delayed time can be :

- ✓ 21 ns
- ✓ 28 ns
- ✓ 35 ns

This signal are in complementary ECL technology (NECL) and there respective pinout are given in annex 10

ORA, ORB : It is the OR of all the signal for a group (ORA for INA and ORB for INB). These outputs are compatible NIM level.
These outputs must be continuously loaded by 50 ohm terminator. If not, the FAST CLEAR output signal can be affected.

MULTA
MULTB

Multiplicity signals associated to a group (MULTA for INA and MULTB for INB).
These signals have amplitude of 50 mV / step under 50 ohms load and **their duration can be adjusted from 16 ns to 134 ns with the front panel potentiometer "MULT WIDTH"**

TRIGA
TRIGB

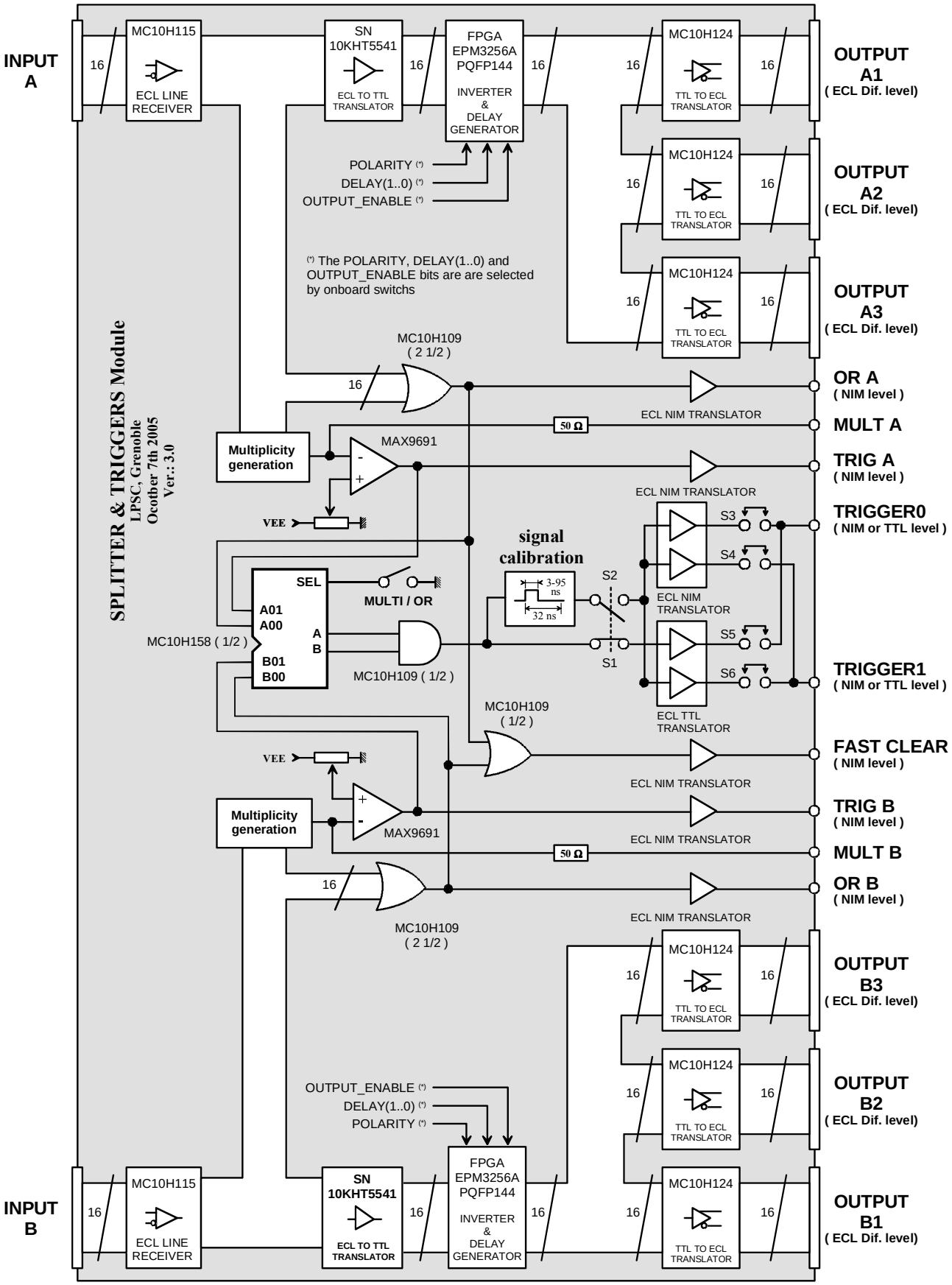
Discriminated Multiplicity (Mult signal > threshold) associated to a group (TRIGA for INA and TRIGB for INB).
These thresholds are regulated by a potentiometer located in the front of the module (one potar for INA and an other for INB). Roughly 2 turns of the potentiometer are equivalent with a multiplicity
These output signals are NIM level compatible.

FAST CLEAR : Corresponds to the OR of ORA and ORB signals.
These output signals are NIM level compatible

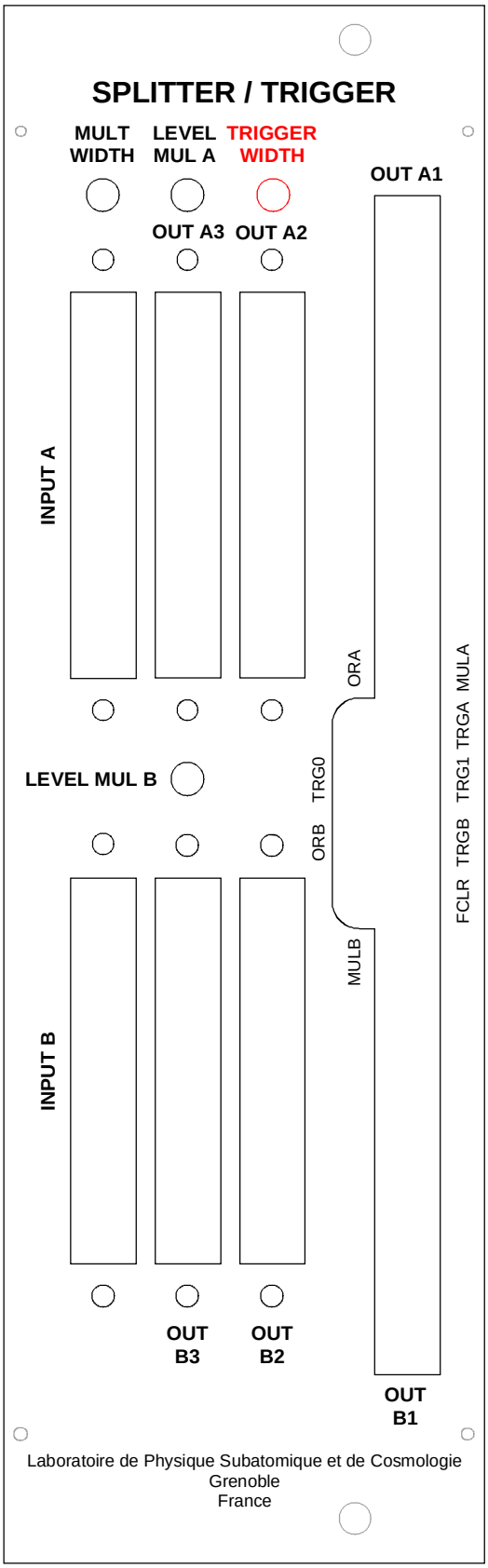
TRIGGER0
TRIGGER1

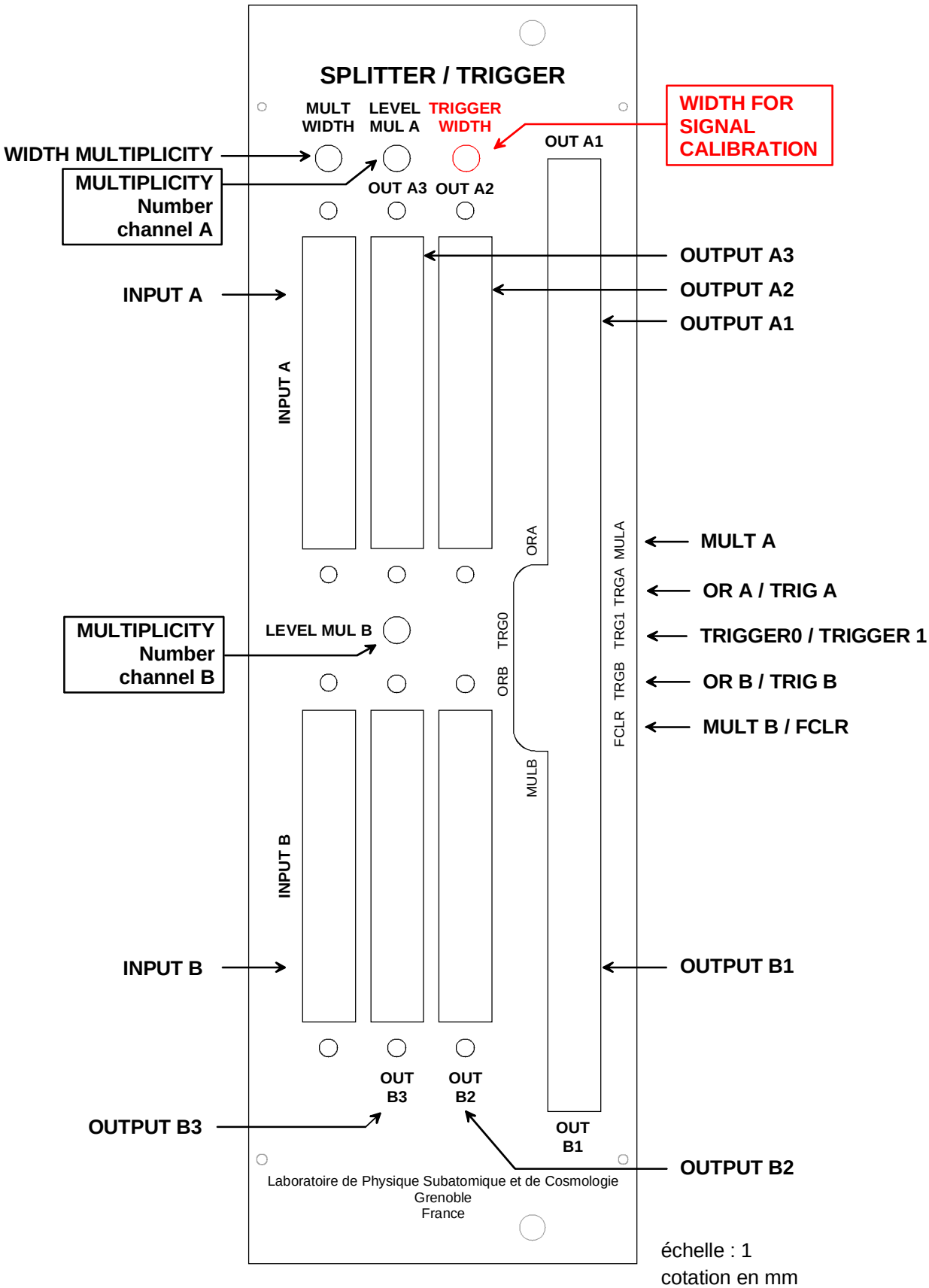
These 2 outputs correspond to the logical AND of the TRIGA with the TRIGB signal.
An internal switch can be used to have or not an adjustable width or directly the width corresponding to the input signals (one switch by output). **The adjustable width lies between 3 and 95 nanosecond.**
Another internal switch can be used to have a NIM or TTL outputs level. The choice can be different for the 2 outputs.

3. « SPLITTER & TRIGGER » board Diagram



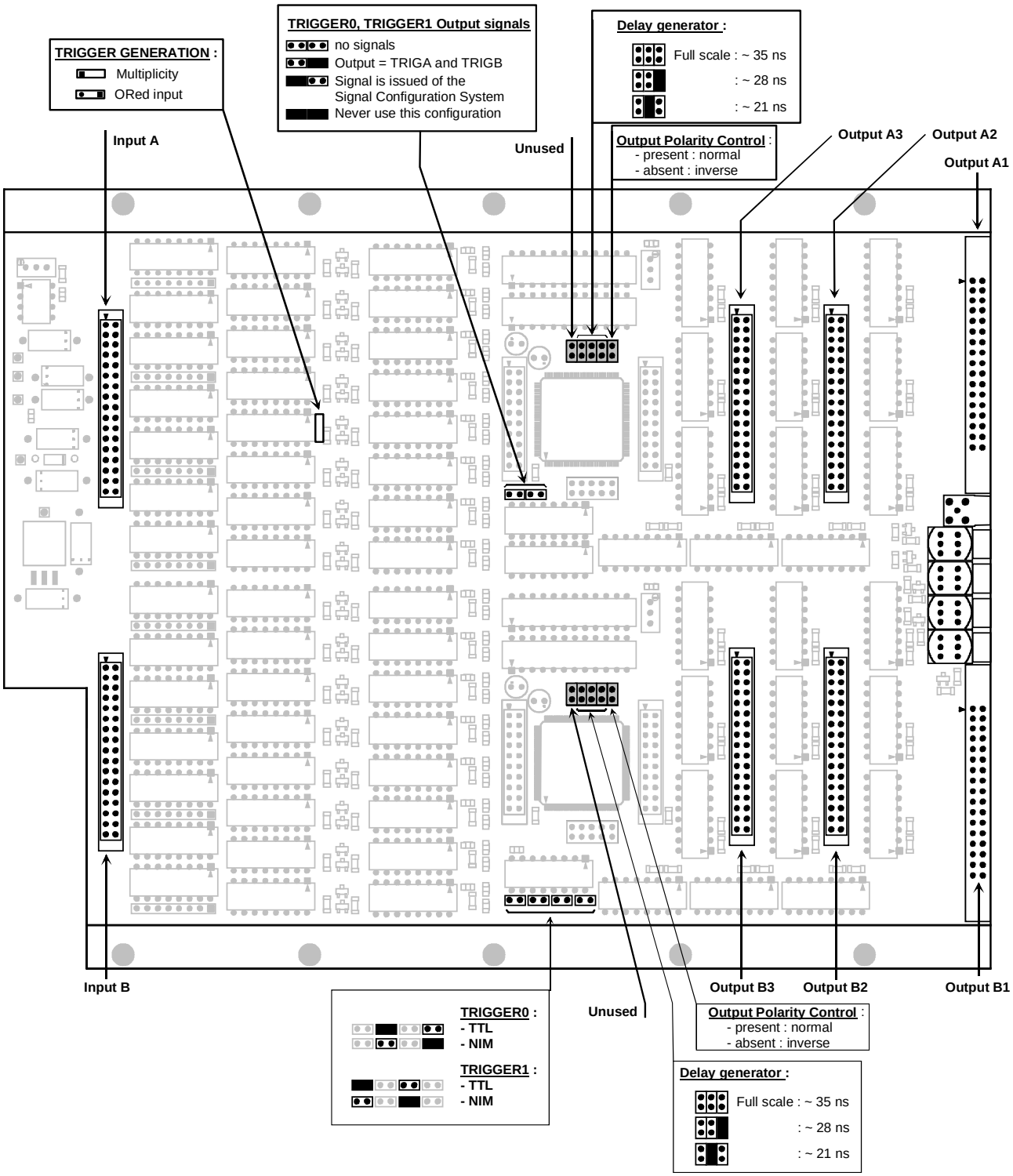
4. « SPLITTER & TRIGGER » Front view





échelle : 1
cotation en mm

5. Switches and setting



6. Board Power consumption

	- 5v	+ 5 v	- 12v	+ 12v
Total max power current :	**6104,91**	1215,00	138,77	16,00
Total typical power current :	**5693,91**	1019,00	128,77	6,00

VCC : 5
VEE : -5
ECL Low level -1,62
ECL high level -0,88
Inside resistor number : 196 ECL Pull down R value (Ω) : 680
Outside resistor number : 192 ECL Pull down R value (Ω) : 680

6.1. Maximum Value :

Designation	Number	Power supply : VEE (- 5,2v)			Power supply : VCC (+ 5v)			Power supply :-12v			Power supply :+12v		
		Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)	Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)	Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)	Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)
MC10H101_dip	17	29	145,00	493,00		0,00	0,00						
MC10H109_dip	6	15	75,00	90,00		0,00	0,00						
MC10H115_dip	8	29	145,00	232,00		0,00	0,00						
MC10H124_dip	24	72	360,00	1728,00	25	125,00	600,00						
SN 10KHT5541_dip	4	33	165,00	132,00	120	600,00	480,00						
MC10H125_dip	1	44	220,00	44,00	63	315,00	63,00						
MC10H131_dip	17	62	310,00	1054,00		0,00	0,00						
MC10192_dip	1	56	280,00	56,00		0,00	0,00						
EPM3256A-10 PQF144	2		0,00	0,00	0	0,00	0,00						
MAX9691	2	36	180,00	72,00	36	180,00	72,00						
NE5532	1		0,00	0,00		0,00	0,00	16		16,00	16		16,00
OP400	2	0	0,00	0,00	0	0,00	0,00						
Mutiplicity Generator	16							0,857		13,71			
NIM generator	7							15,58		109,06			
			Subtotal :	**3901,00**		Subtotal :	1215,00			138,77			16,00
Inside pull down resistor													
worst case :	253	6,06	0,025	1532,88									
best case :	135	4,97	0,017	671,03									
			Subtotal :	**2203,91**									
			Subtotal :	**6104,91**									

6.2. Typical Value :

Typical Value

Designation	Number	Power supply : VEE (- 5,2v)			Power supply : VCC (+ 5v)			Power supply :-12v			Power supply :+12v		
		Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)	Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)	Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)	Power Current (mA)	Chip consumption (mW)	Total Power Current (mA)
MC10H101_dip	17	26	130,00	442,00		0,00	0,00						
MC10H109_dip	6	14	70,00	84,00		0,00	0,00						
MC10H115_dip	8	26	130,00	208,00		0,00	0,00						
MC10H124_dip	24	66	330,00	1584,00	25	125,00	600,00						
SN 10KHT5541_dip	4	22	110,00	88,00	80	400,00	320,00						
MC10H125_dip	1	40	200,00	40,00	63	315,00	63,00						
MC10H131_dip	17	56	280,00	952,00		0,00	0,00						
MC10192_dip	1	56	280,00	56,00		0,00	0,00						
EPM3256A-10 PQF144	2		0,00	0,00		0,00	0,00						
MAX9691	2	18	90,00	36,00	18	90,00	36,00						
NE5532	1		0,00	0,00		0,00	0,00	6		6,00	6		6,00
OP400	2	0	0,00	0,00	0	0,00	0,00						
Mutiplicity Generator	16							0,857		13,71			
NIM generator	7							15,58		109,06			
			Subtotal :	3490,00		Subtotal :	1019,00			128,77			6,00
Inside pull down resistor													
worst case :	253	6,06	0,025	1532,88									
best case :	135	4,97	0,017	671,03									
			Subtotal :	**2203,91**									
			Total power current :	5693,91									

7. DELAY_50 Component

7.1. EPM3256A I/O and dedicated Pin-outs

EPM3256A (144-PinTQFP)			
Dedicated Pin		LAB	
INPUT/GCLK1	125	A	1, 2, 139, 140, 141, 142, 143
INPUT/GCLRn	127	B	4[1],5, 6, 7, 8, 9, 10
INPUT/OE1	126	C	28, 29, 30, 31, 32, 34, 35, 36
INPUT/OE2/GCLK2	128	D	37, 38, 39, 40, 41, 42, 43, 44
TDI [1]	4	E	131, 132, 133, 134, 136, 137, 138
TMS [1]	20	F	11, 12, 14, 15, 16, 18, 19
TCK [1]	89	G	20(1), 21, 22, 23, 25, 27
TDO [1]	104	H	45, 46, 47, 48, 49, 53, 54
GNDINT	52, 57, 124, 129	I	116, 117, 118, 119, 120, 121, 122
GNDIO	3, 13, 17, 26, 33, 59, 64, 77, 85, 94, 105, 114, 135	J	90, 91, 92, 93, 96, 97
VCCINT (3.3 V Only)	51, 58, 123, 130	K	82, 83, 84, 86, 87, 88, 89[1]
VCCIO (2.5 V or 3.3 V)	24, 50, 73, 76, 95, 115, 144	L	55, 56, 60, 61, 62, 63, 65
		M	106, 107, 108, 109, 110, 111, 112, 113
		N	98, 99, 100, 101, 102, 103, 104[1]
		O	74, 75, 78, 79, 80, 81
		P	66, 67, 68, 69, 70, 71, 72

[1] This pin may function as either a JTAG port or a user I/O pin. When the device is configured to use the JTAG ports for insystem programming, this pin is not available as a user I/O pin.

7.2. « DELAY_50 » Component pin report

Pin Name	Loc.	Dir.	I/O level	Volt.
Signal_in_a[13]	1	bidir	LVTTL	
signal_in_a[14]	2	bidir	LVTTL	
GND	3	gnd		
TDI	4	input	LVTTL	
signal_in_a[6]	5	bidir	LVTTL	
signal_in_a[7]	6	bidir	LVTTL	
signal_in_a[8]	7	bidir	LVTTL	
signal_in_a[10]	8	bidir	LVTTL	
signal_in_a[11]	9	bidir	LVTTL	
signal_in_a[9]	10	bidir	LVTTL	
signal_in_b[11]	11	bidir	LVTTL	
signal_in_b[10]	12	bidir	LVTTL	
GND	13	gnd		
signal_in_b[9]	14	bidir	LVTTL	
signal_in_b[8]	15	bidir	LVTTL	
signal_in_b[7]	16	bidir	LVTTL	
GND	17	gnd		
signal_in_b[6]	18	bidir	LVTTL	

Pin Name	Loc.	Dir.	I/O level	Volt.
signal_in_b[5]	19	bidir	LVTTL	
TMS	20	input	LVTTL	
signal_in_b[0]	21	bidir	LVTTL	
signal_in_b[1]	22	bidir	LVTTL	
signal_in_b[2]	23	bidir	LVTTL	
VCCIO	24	power		3.3V
signal_in_b[3]	25	bidir	LVTTL	
GND	26	gnd		
signal_in_b[4]	27	bidir	LVTTL	
signal_in_a[4]	28	bidir	LVTTL	
signal_in_a[5]	29	bidir	LVTTL	
signal_in_a[3]	30	bidir	LVTTL	
signal_in_b[14]	31	bidir	LVTTL	
signal_in_b[15]	32	bidir	LVTTL	
GND	33	gnd		
signal_in_a[0]	34	bidir	LVTTL	
signal_in_a[1]	35	bidir	LVTTL	
signal_in_a[2]	36	bidir	LVTTL	
signal_in_c[13]	37	bidir	LVTTL	

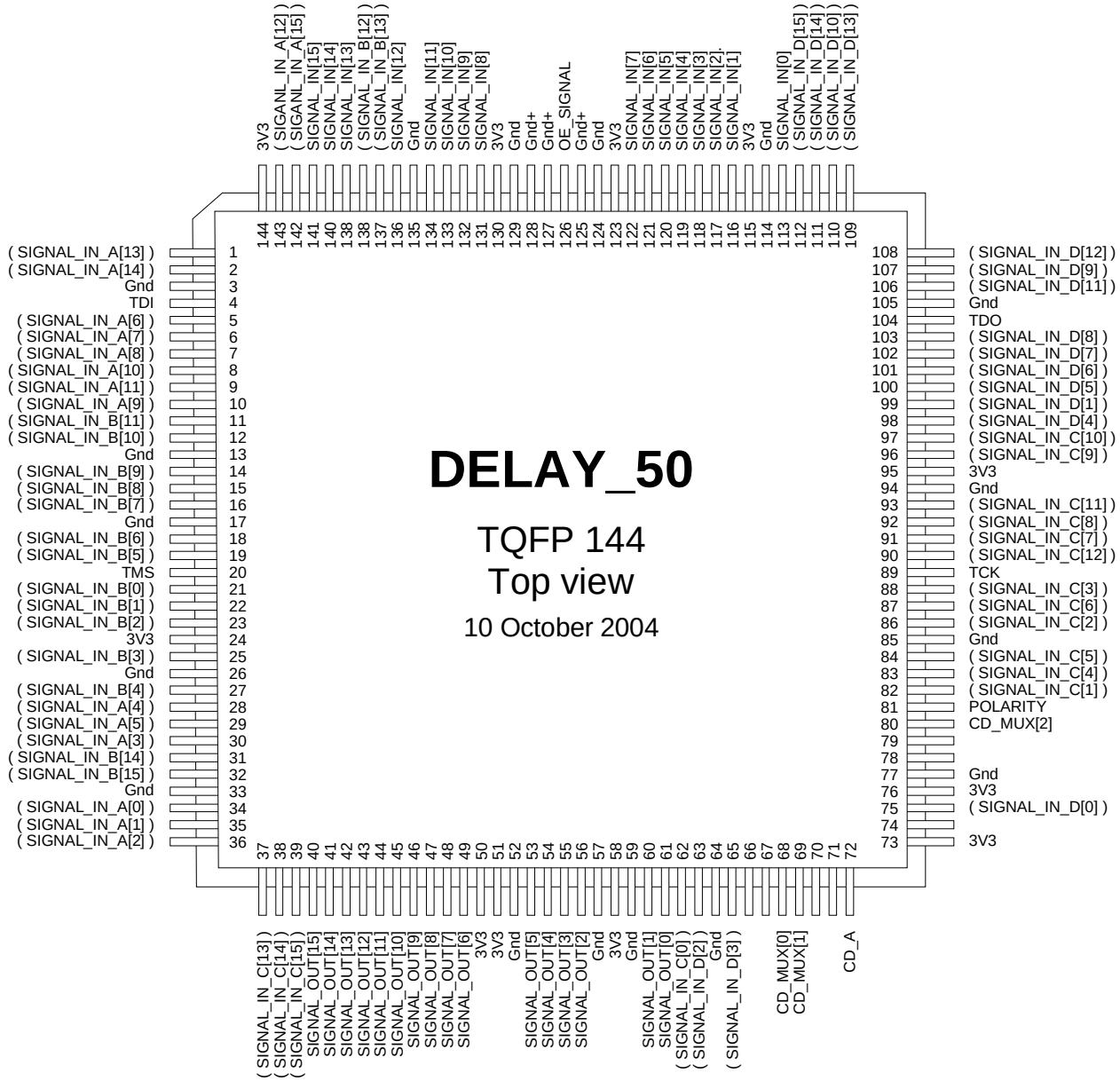
Pin Name	Loc.	Dir.	I/O level	Volt.
signal_in_c[14]	38	bidir	LVTTL	
signal_in_c[15]	39	bidir	LVTTL	
signal_out[15]	40	output	LVTTL	
signal_out[14]	41	output	LVTTL	
signal_out[13]	42	output	LVTTL	
signal_out[12]	43	output	LVTTL	
signal_out[11]	44	output	LVTTL	
signal_out[10]	45	output	LVTTL	
signal_out[9]	46	output	LVTTL	
signal_out[8]	47	output	LVTTL	
signal_out[7]	48	output	LVTTL	
signal_out[6]	49	output	LVTTL	
VCCIO	50	power		3.3V
VCCINT	51	power		3.3V
GND	52	gnd		
signal_out[5]	53	output	LVTTL	
signal_out[4]	54	output	LVTTL	
signal_out[3]	55	output	LVTTL	
signal_out[2]	56	output	LVTTL	
GND	57	gnd		
VCCINT	58	power		3.3V
GND	59	gnd		
signal_out[1]	60	output	LVTTL	
signal_out[0]	61	output	LVTTL	
signal_in_c[0]	62	bidir	LVTTL	
signal_in_d[2]	63	bidir	LVTTL	
GND	64	gnd		
signal_in_d[3]	65	bidir	LVTTL	
RESERVED	66			
RESERVED	67			
cd_mux[0]	68	input	LVTTL	
cd_mux[1]	69	input	LVTTL	
RESERVED	70			
RESERVED	71			
CD_A	72	input	LVTTL	
VCCIO	73	power		3.3V
RESERVED	74			
signal_in_d[0]	75	bidir	LVTTL	
VCCIO	76	power		3.3V
GND	77	gnd		
RESERVED	78			
RESERVED	79			
cd_mux[2]	80	input	LVTTL	
POLARITY	81	input	LVTTL	
signal_in_c[1]	82	bidir	LVTTL	
signal_in_c[4]	83	bidir	LVTTL	
signal_in_c[5]	84	bidir	LVTTL	
GND	85	gnd		
signal_in_c[2]	86	bidir	LVTTL	

Pin Name	Loc.	Dir.	I/O level	Volt.
signal_in_c[6]	87	bidir	LVTTL	
signal_in_c[3]	88	bidir	LVTTL	
TCK	89	input	LVTTL	
signal_in_c[12]	90	bidir	LVTTL	
signal_in_c[7]	91	bidir	LVTTL	
signal_in_c[8]	92	bidir	LVTTL	
signal_in_c[11]	93	bidir	LVTTL	
GND	94	gnd		
VCCIO	95	power		3.3V
signal_in_c[9]	96	bidir	LVTTL	
signal_in_c[10]	97	bidir	LVTTL	
signal_in_d[4]	98	bidir	LVTTL	
signal_in_d[1]	99	bidir	LVTTL	
signal_in_d[5]	100	bidir	LVTTL	
signal_in_d[6]	101	bidir	LVTTL	
signal_in_d[7]	102	bidir	LVTTL	
signal_in_d[8]	103	bidir	LVTTL	
TDO	104	output	LVTTL	
GND	105	gnd		
signal_in_d[11]	106	bidir	LVTTL	
signal_in_d[9]	107	bidir	LVTTL	
signal_in_d[12]	108	bidir	LVTTL	
signal_in_d[13]	109	bidir	LVTTL	
signal_in_d[10]	110	bidir	LVTTL	
signal_in_d[14]	111	bidir	LVTTL	
signal_in_d[15]	112	bidir	LVTTL	
signal_in[0]	113	input	LVTTL	
GND	114	gnd		
VCCIO	115	power		3.3V
signal_in[1]	116	input	LVTTL	
signal_in[2]	117	input	LVTTL	
signal_in[3]	118	input	LVTTL	
signal_in[4]	119	input	LVTTL	
signal_in[5]	120	input	LVTTL	
signal_in[6]	121	input	LVTTL	
signal_in[7]	122	input	LVTTL	
VCCINT	123	power		3.3V
GND	124	gnd		
GND+	125			
oe_signal	126	input	LVTTL	
GND+	127			
GND+	128			
GND	129	gnd		
VCCINT	130	power		3.3V
signal_in[8]	131	input	LVTTL	
signal_in[9]	132	input	LVTTL	
signal_in[10]	133	input	LVTTL	
signal_in[11]	134	input	LVTTL	
GND	135	gnd		

Pin Name	Loc.	Dir.	I/O level	Volt.
signal_in[12]	136	input	LVTTL	
signal_in_b[13]	137	bidir	LVTTL	
signal_in_b[12]	138	bidir	LVTTL	
signal_in[13]	139	input	LVTTL	
signal_in[14]	140	input	LVTTL	

Pin Name	Loc.	Dir.	I/O level	Volt.
signal_in[15]	141	input	LVTTL	
signal_in_a[15]	142	bidir	LVTTL	
signal_in_a[12]	143	bidir	LVTTL	
VCCIO	144	power		3.3V

7.3. « DELAY_50 » Component Pinout

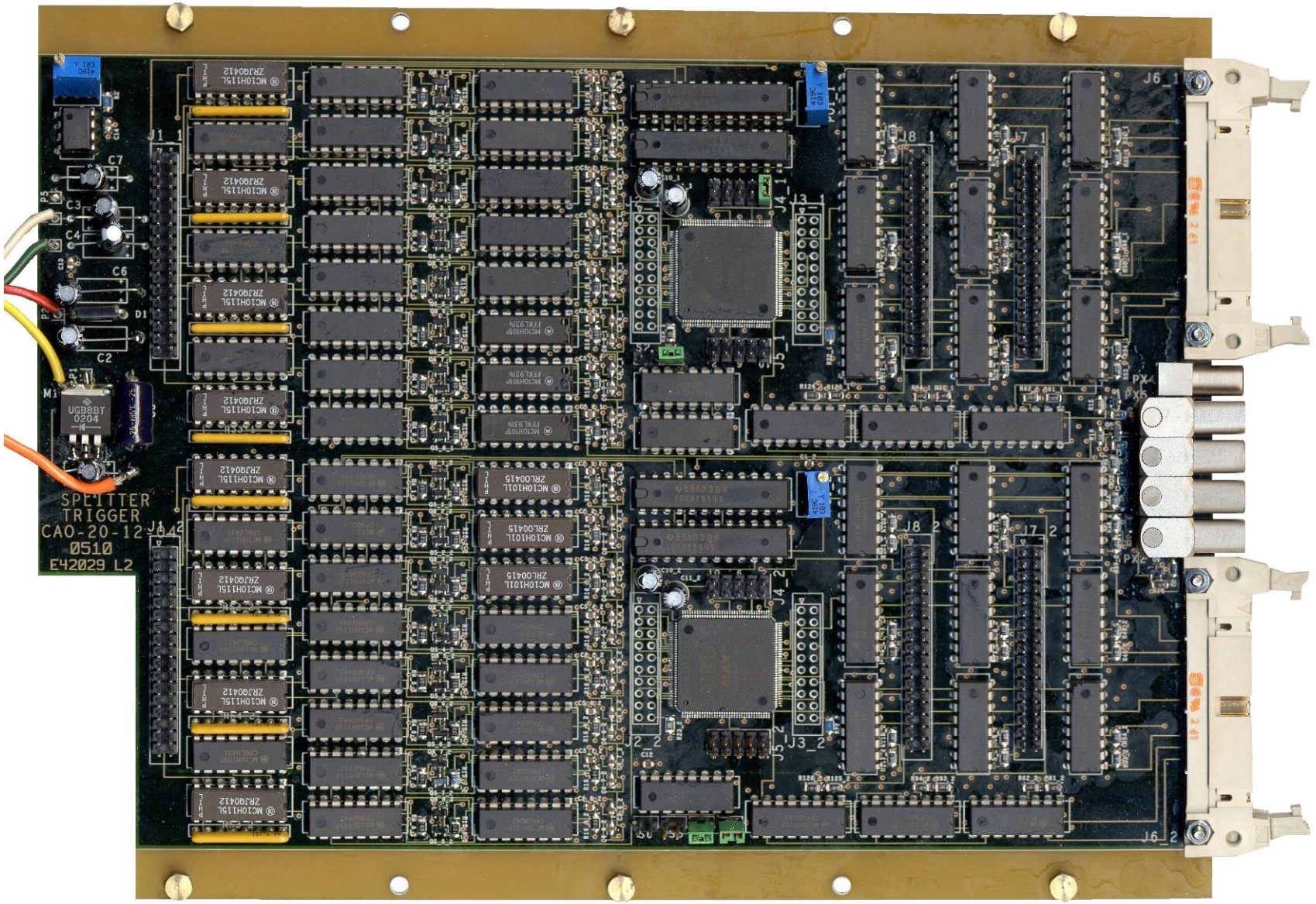


7.4. « DELAY_50 » VHDL description

```
--============================================================================
--
-- Design Units : G0 experiment
--
-- File name    : delay.vhd
--
-- Purpose      : This CPLD generate a delay ( 10 to 50 ns ) on a 16 bit data bus.
--
-- Notes        :
--
-- Limitations  :
--
-- Errors       :
--
-- Library      :
--
-- Dependencies :
--
-- Author       : Joel BOUVIER
--                Laboratoire de physique Subatomique et de cosmologie
--                53 Avenue des Martyrs
--                38026 Grenoble Cedex, FRANCE
--
--============================================================================
-- Revision List
-- 2.0       31/03/2005   The polarity of the “polarity” signal are inverted
-- 1.0       17/09/2004   delay is encreased to 50 ns
-- 0.0       08/09/2004   Initial version ( delay 10 to 30 ns )
--============================================================================

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.”+”;

entity DELAY is
  generic ( bus_width : natural :=15 );

  port (
    POLARITY    : in    std_logic ;                       -- Control input polarity
    signal_in   : in    std_logic_vector(bus_width downto 0);-- Data in

    CD_A        : in    std_logic ;                       -- Must be connect to 0
    signal_in_a : inout std_logic_vector(bus_width downto 0);-- Intermediary signal
    signal_in_b : inout std_logic_vector(bus_width downto 0);-- Intermediary signal
    signal_in_c : inout std_logic_vector(bus_width downto 0);-- Intermediary signal
    signal_in_d : inout std_logic_vector(bus_width downto 0);-- Intermediary signal

    cd_mux      : in    std_logic_vector(2 downto 0);     -- Ouput Delay signals
    oe_signal   : in    std_logic ;                       -- Output is ‘Z’ when ‘0’
```

```
    signal_out  : out   std_logic_vector(bus_width downto 0) ); -- Output signal
end DELAY ;

architecture behave of DELAY is
 signal signal_int     : std_logic_vector(bus_width downto 0);
 signal signal_out_int : std_logic_vector(bus_width downto 0);
begin

 signal_int  <= signal_in   when POLARITY ='0' else ( not signal_in );
 signal_in_a <= signal_int  when CD_A ='0'     else ( others => 'Z' );
 signal_in_b <= signal_in_a when cd_mux(2) ='1'     else ( others => 'Z' );
 signal_in_c <= signal_in_b when cd_mux(1) ='1'     else ( others => 'Z' );
 signal_in_d <= signal_in_c when cd_mux(0) ='1'     else ( others => 'Z' );

 signal_out_int <= signal_in_d when cd_mux = "111" else
                   signal_in_c when cd_mux = "110" else
                   signal_in_b ;

 signal_out <= signal_out_int when oe_signal = '0' else  ( others => 'Z' );

end behave ;
```

Annex 1 : board picture

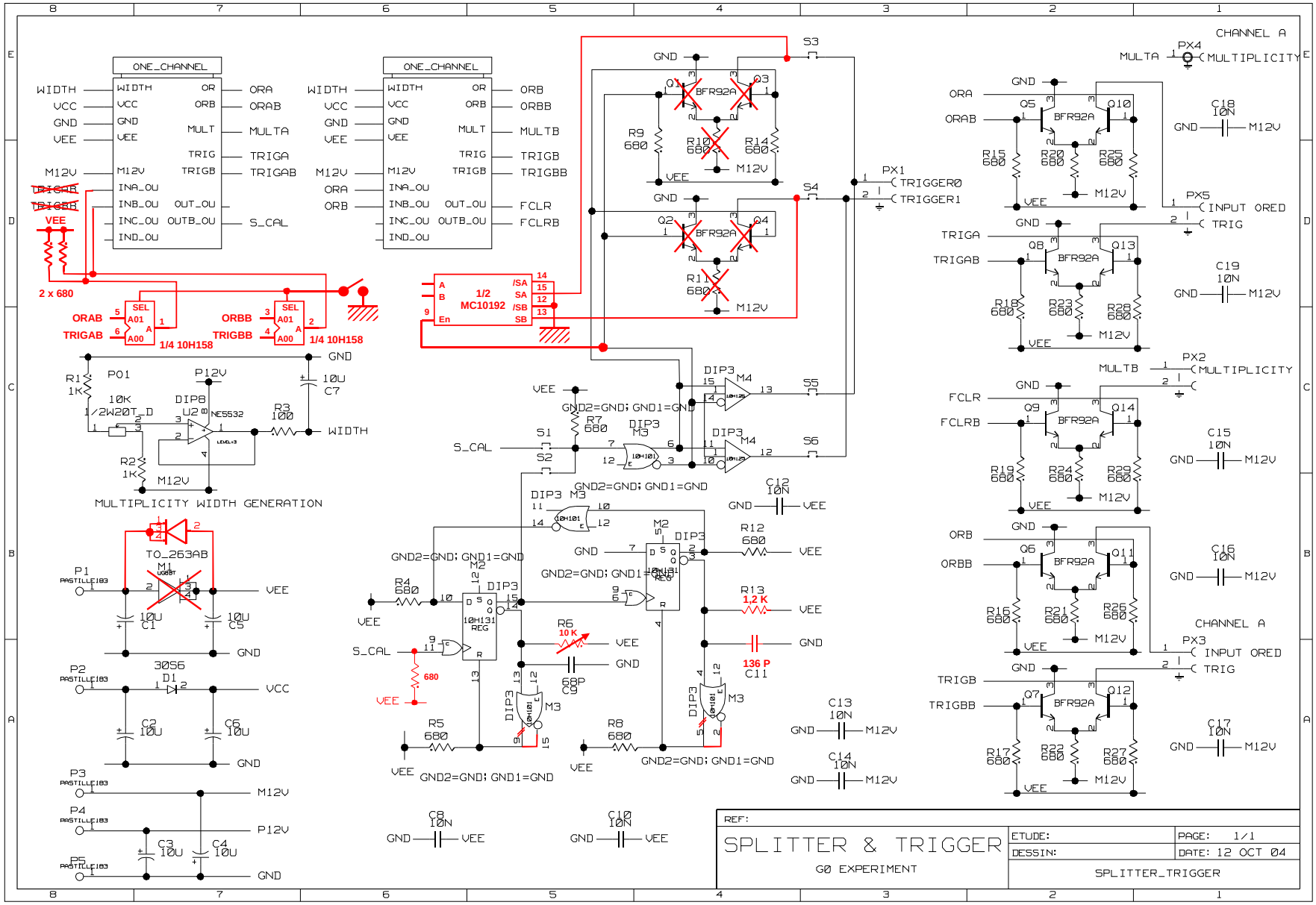


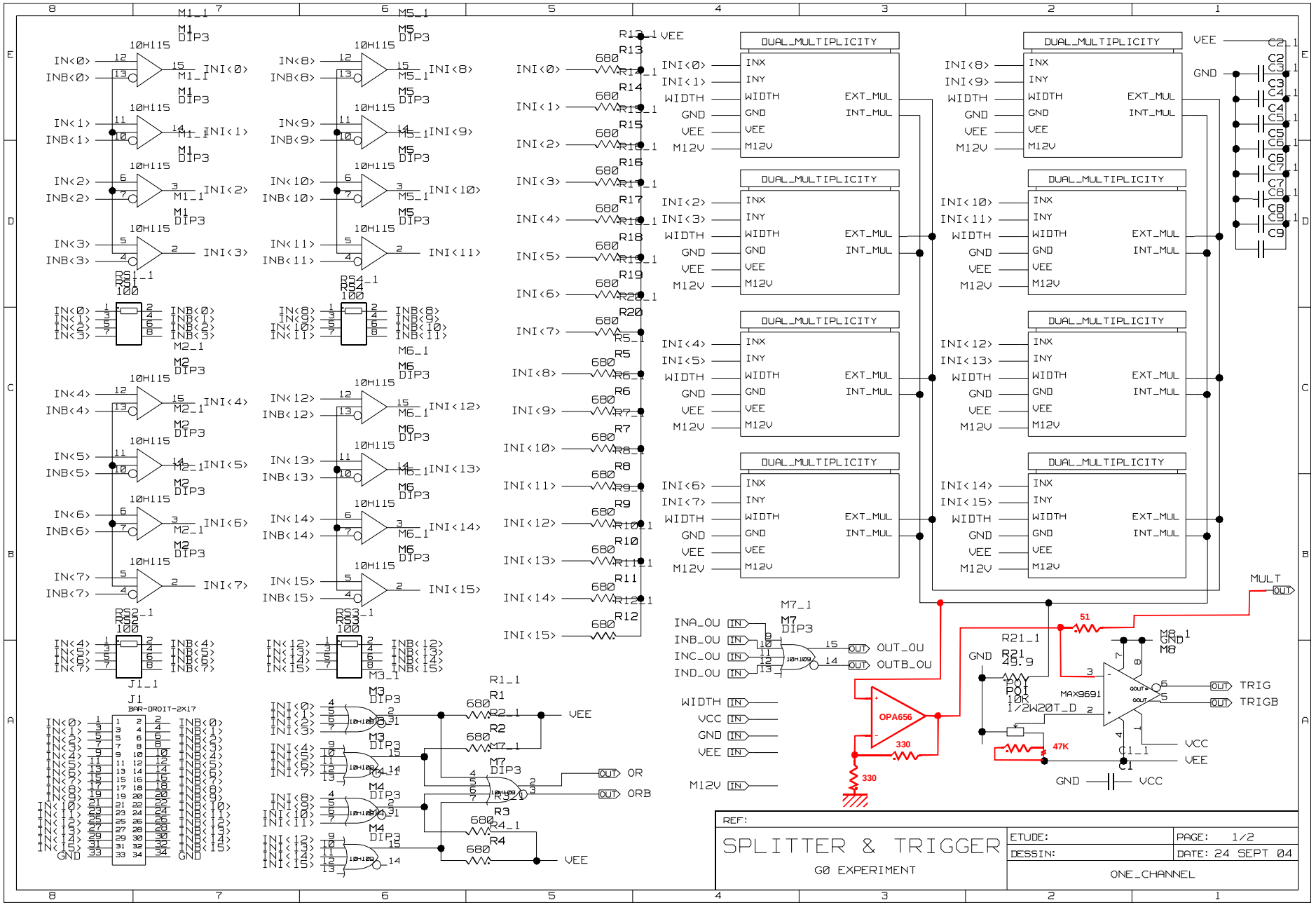
Annex 2 : Generic pinout connector

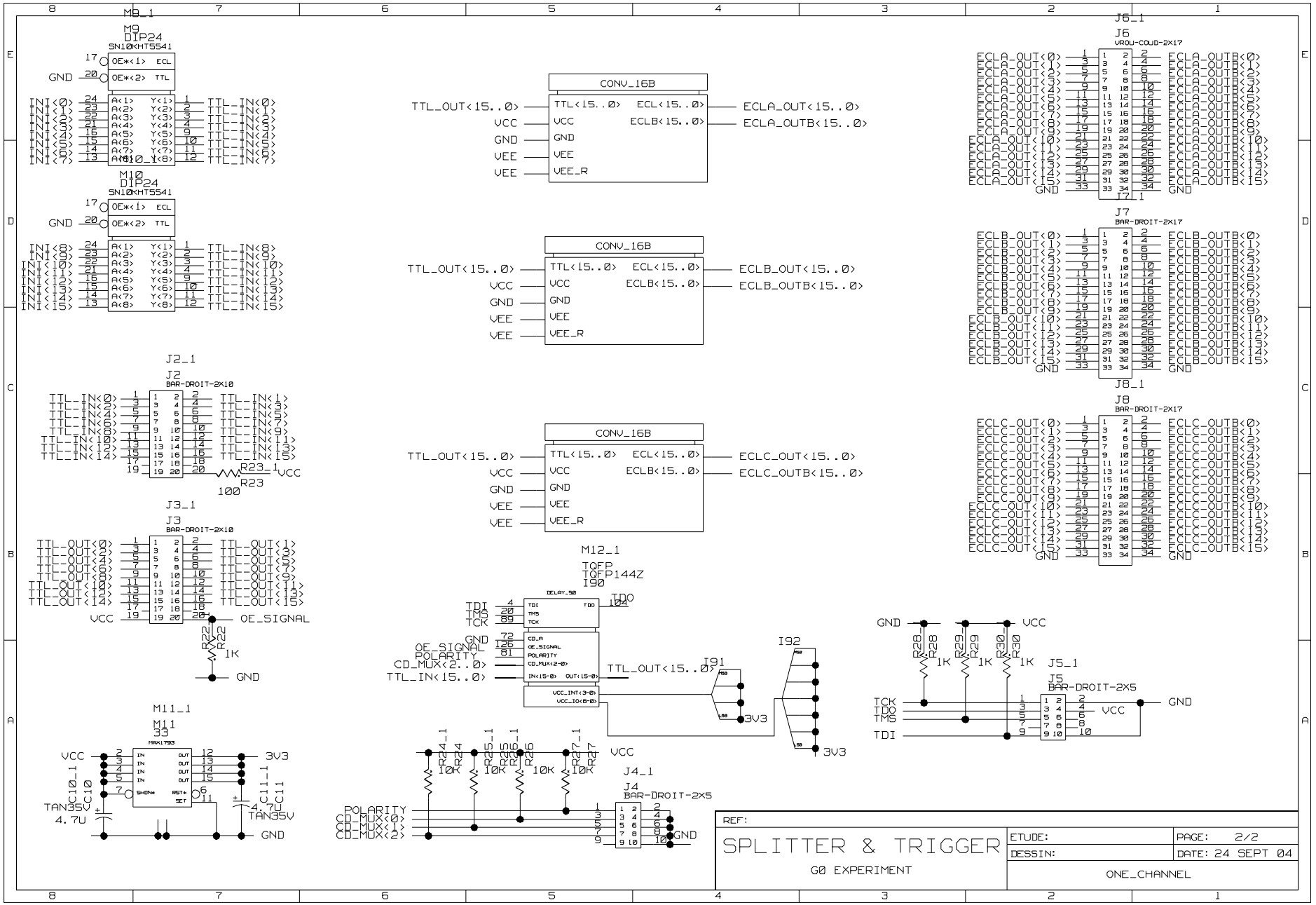
designation	Name	Pin	pin	Name	designation
Input 0 (positive polarity)	INA[0]+	1	2	INA[0]-	Input 0 (negative polarity)
Input 1 (positive polarity)	INA[1]+	3	4	INA[1]-	Input 1 (negative polarity)
Input 2 (positive polarity)	INA[2]+	5	6	INA[2]-	Input 2 (negative polarity)
Input 3 (positive polarity)	INA[3]+	7	8	INA[3]-	Input 2 (negative polarity)
Input 4 (positive polarity)	INA[4]+	9	10	INA[4]-	Input 4 (negative polarity)
Input 5 (positive polarity)	INA[5]+	11	12	INA[5]-	Input 5 (negative polarity)
Input 6 (positive polarity)	INA[6]+	13	14	INA[6]-	Input 6 (negative polarity)
Input 7 (positive polarity)	INA[7]+	15	16	INA[7]-	Input 7 (negative polarity)
Input 8 (positive polarity)	INA[8]+	17	18	INA[8]-	Input 8 (negative polarity)
Input 9 (positive polarity)	INA[9]+	19	20	INA[9]-	Input 9 (negative polarity)
Input 10 (positive polarity)	INA[10]+	21	22	INA[10]-	Input 10 (negative polarity)
Input 11 (positive polarity)	INA[11]+	23	24	INA[11]-	Input 11 (negative polarity)
Input 12 (positive polarity)	INA[12]+	25	26	INA[12]-	Input 12 (negative polarity)
Input 13 (positive polarity)	INA[13]+	27	28	INA[13]-	Input 13 (negative polarity)
Input 14 (positive polarity)	INA[14]+	29	30	INA[14]-	Input 14 (negative polarity)
Input 15 (positive polarity)	INA[15]+	31	32	INA[15]-	Input 15 (negative polarity)
	Gnd	33	34	Gnd	

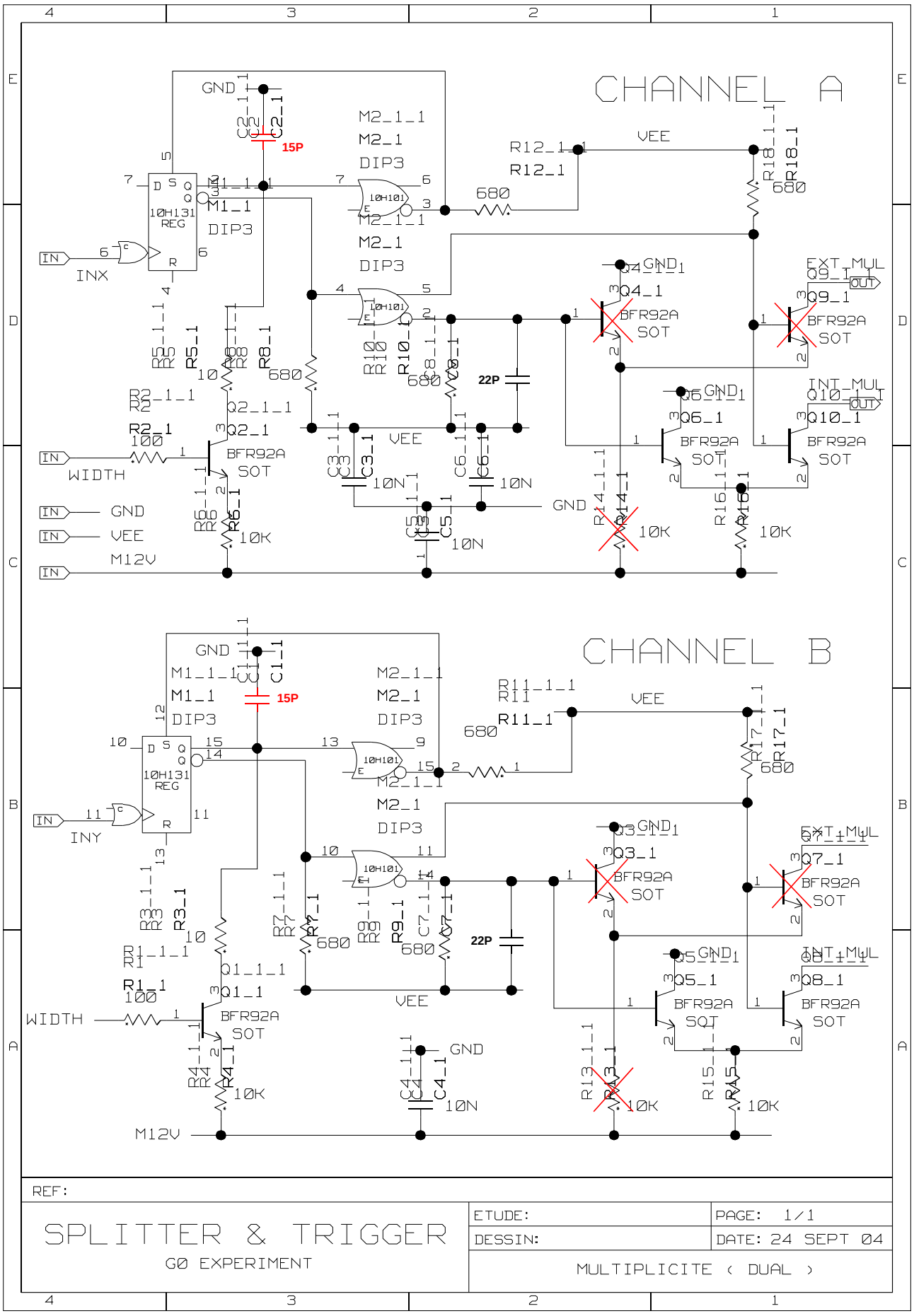
designation	Name	Pin	pin	Name	designation
Input 0 (positive polarity)	OUTA[0]+	1	2	OUTA[0]-	Input 0 (negative polarity)
Input 1 (positive polarity)	OUTA[1]+	3	4	OUTA[1]-	Input 1 (negative polarity)
Input 2 (positive polarity)	OUTA[2]+	5	6	OUTA[2]-	Input 2 (negative polarity)
Input 3 (positive polarity)	OUTA[3]+	7	8	OUTA[3]-	Input 3 (negative polarity)
Input 4 (positive polarity)	OUTA[4]+	9	10	OUTA[4]-	Input 4 (negative polarity)
Input 5 (positive polarity)	OUTA[5]+	11	12	OUTA[5]-	Input 5 (negative polarity)
Input 6 (positive polarity)	OUTA[6]+	13	14	OUTA[6]-	Input 6 (negative polarity)
Input 7 (positive polarity)	OUTA[7]+	15	16	OUTA[7]-	Input 7 (negative polarity)
Input 8 (positive polarity)	OUTA[8]+	17	18	OUTA[8]-	Input 8 (negative polarity)
Input 9 (positive polarity)	OUTA[9]+	19	20	OUTA[9]-	Input 9 (negative polarity)
Input 10 (positive polarity)	OUTA[10]+	21	22	OUTA[10]-	Input 10 (negative polarity)
Input 11 (positive polarity)	OUTA[11]+	23	24	OUTA[11]-	Input 11 (negative polarity)
Input 12 (positive polarity)	OUTA[12]+	25	26	OUTA[12]-	Input 12 (negative polarity)
Input 13 (positive polarity)	OUTA[13]+	27	28	OUTA[13]-	Input 13 (negative polarity)
Input 14 (positive polarity)	OUTA[14]+	29	30	OUTA[14]-	Input 14 (negative polarity)
Input 15 (positive polarity)	OUTA[15]+	31	32	OUTA[15]-	Input 15 (negative polarity)
	Gnd	33	34	Gnd	

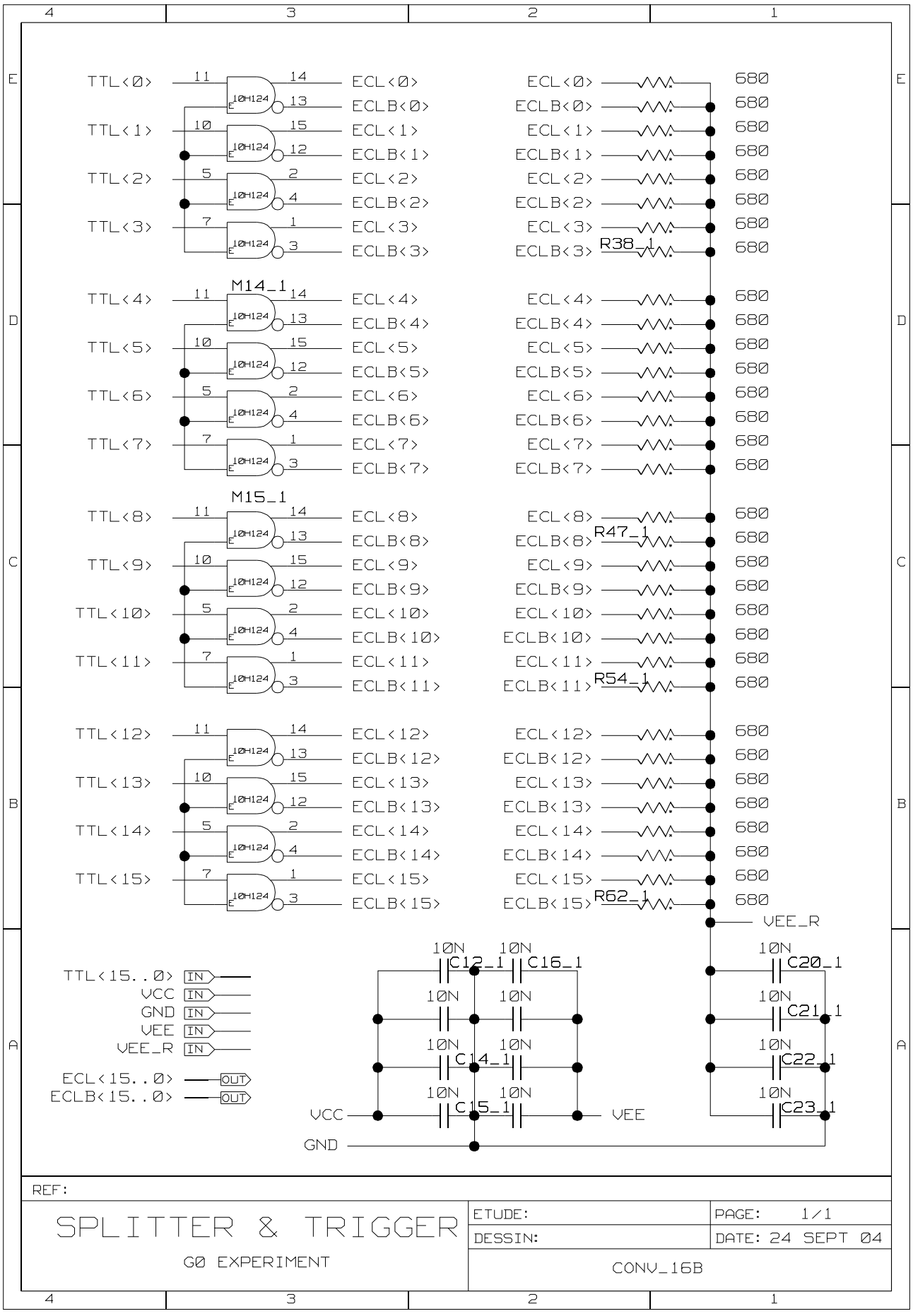
Annex 3 : Board scheme




SPLITTER & TRIGGER
G0 EXPERIMENT
REF:
ETUDE:
DESSIN:
PAGE: 1/2
DATE: 24 SEPT 04
ONE_CHANNEL
DUAL_MULTIPLICITY
INX
INY
WIDTH
GND
VEE
M12V
EXT_MUL
INT_MUL
10H115
DIP3
BAR-DROIT-2X17
OPA656
MAX9691
MULT
TRIG
TRIGB
OR
ORB
OUT_OU
OUTB_OU
VCC


M9
DIP24
SN10KHT5541
M10
DIP24
SN10KHT5541
CONV_16B
TTL_OUT<15..0>
ECLA_OUT<15..0>
ECLA_OUTB<15..0>
ECLB_OUT<15..0>
ECLB_OUTB<15..0>
ECLC_OUT<15..0>
ECLC_OUTB<15..0>
J6
J7
J8
J2
J3
R23
100
VCC
GND
OE_SIGNAL
M12_1
TQFP
TQFP144Z
I90
I91
I92
3V3
R22
1K
R24
R25
R26
R27
10K
J4
J5
BAR-DROIT-2X5
M11
MAX793
C10
C11
4.7U
TAN35V
TCK
TDO
TMS
TDI
POLARITY
CD_MUX<0>
CD_MUX<1>
CD_MUX<2>
R28
R29
R30
REF:
SPLITTER & TRIGGER
G0 EXPERIMENT
ETUDE:
DESSIN:
PAGE: 2/2
DATE: 24 SEPT 04
ONE_CHANNEL


CHANNEL A
CHANNEL B
GND
VEE
M12V
IN
INX
INY
WIDTH
15P
22P
10N
10K
680
100
10
M1_1
M2_1
DIP3
10H131
REG
10H101
BFR92A
SOT
EXT_MUL
INT_MUL
OUT
REF:
SPLITTER & TRIGGER
G0 EXPERIMENT
ETUDE:
DESSIN:
PAGE: 1/1
DATE: 24 SEPT 04
MULTIPLICITE (DUAL)


4
3
2
1
E
D
C
B
A
TTL<0>
TTL<1>
TTL<2>
TTL<3>
TTL<4>
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TTL<6>
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TTL<11>
TTL<12>
TTL<13>
TTL<14>
TTL<15>
10H124
M14_1
M15_1
ECL<0>
ECLB<0>
ECL<1>
ECLB<1>
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ECL<3>
ECLB<3>
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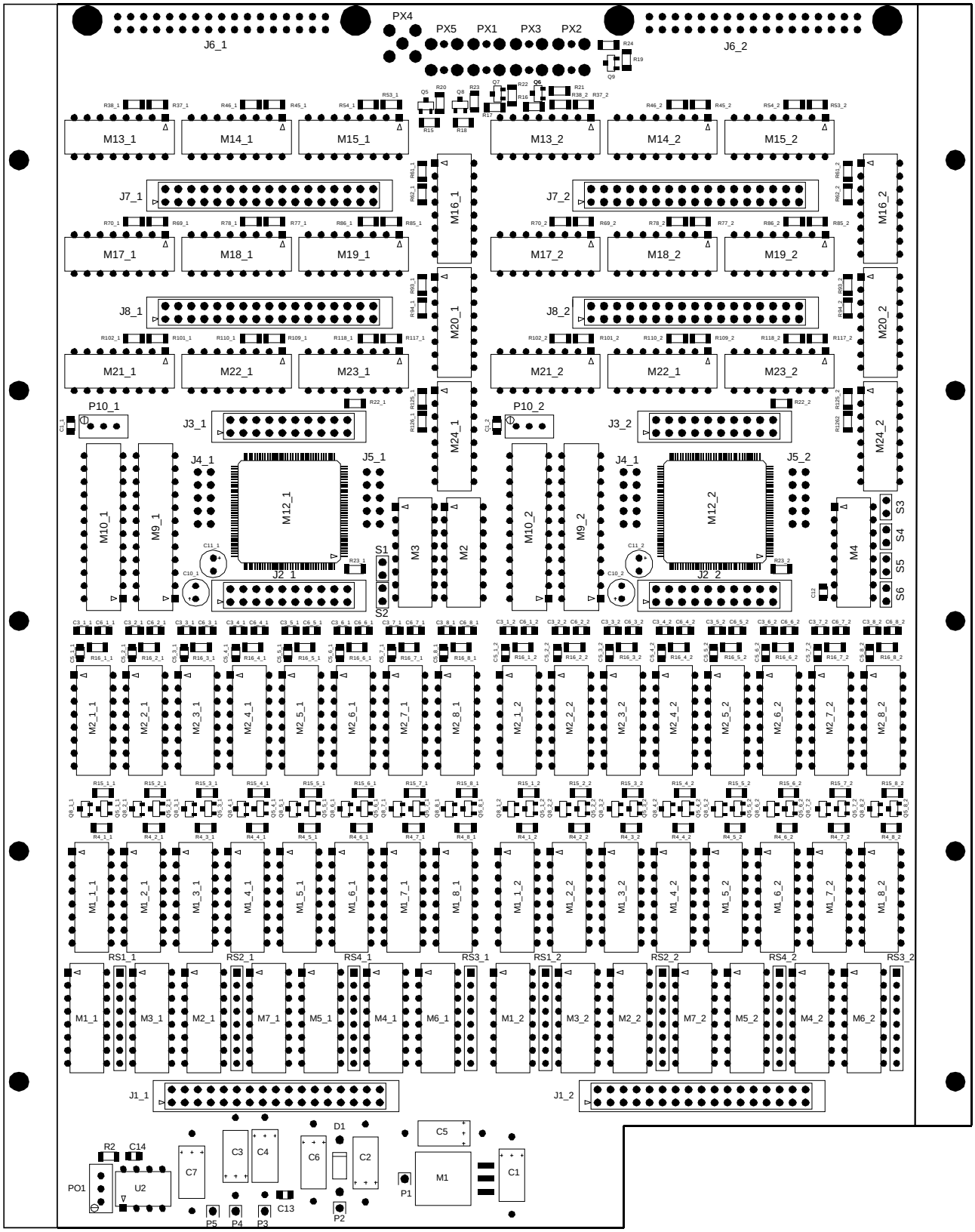
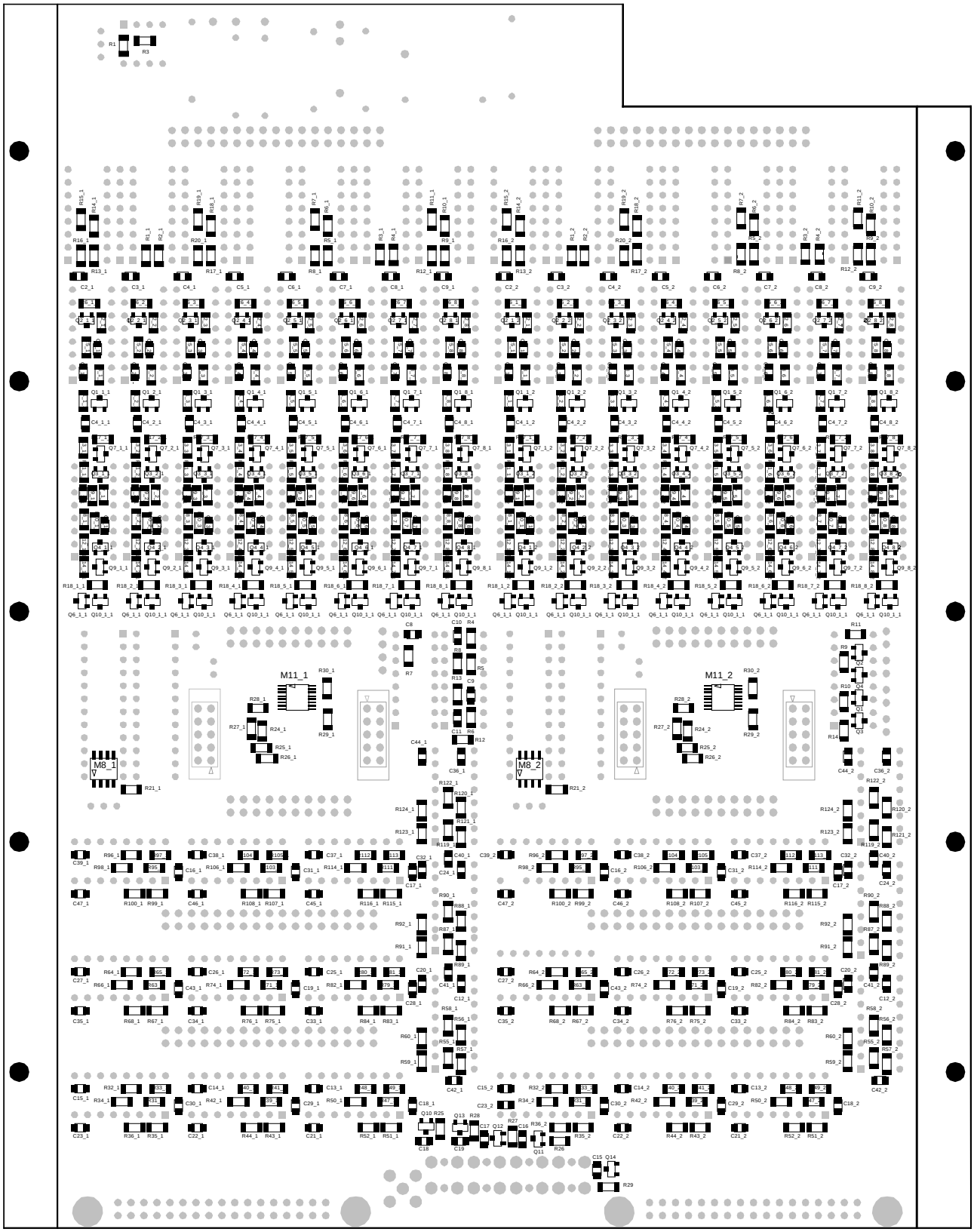
ECLB<12>
ECL<13>
ECLB<13>
ECL<14>
ECLB<14>
ECL<15>
ECLB<15>
680
R38_1
R47_1
R54_1
R62_1
VEE_R
10N
C12_1
C16_1
C20_1
C21_1
C14_1
C22_1
C15_1
C23_1
VCC
VEE
GND
TTL<15..0>
VCC
GND
VEE
VEE_R
ECL<15..0>
ECLB<15..0>
IN
OUT
REF:
SPLITTER & TRIGGER
G0 EXPERIMENT
ETUDE:
PAGE: 1/1
DESSIN:
DATE: 24 SEPT 04
CONV_16B

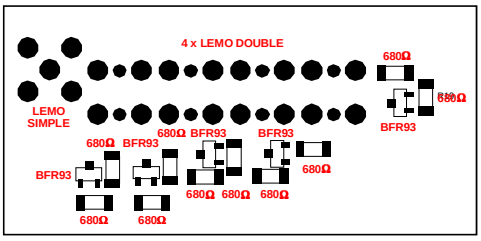
Annex 4 : board representation (component side)

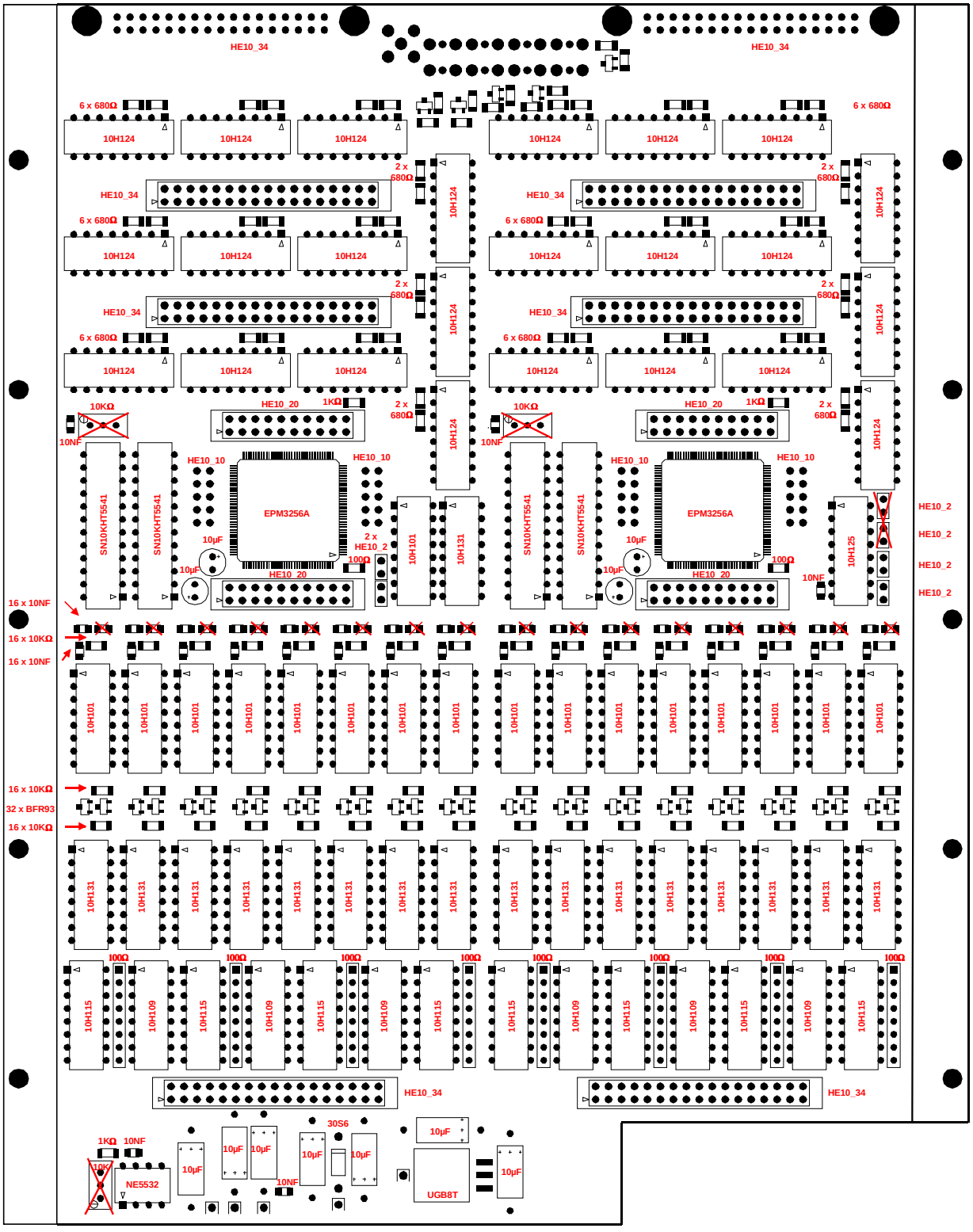


Annex 5 : board representation (sold side)

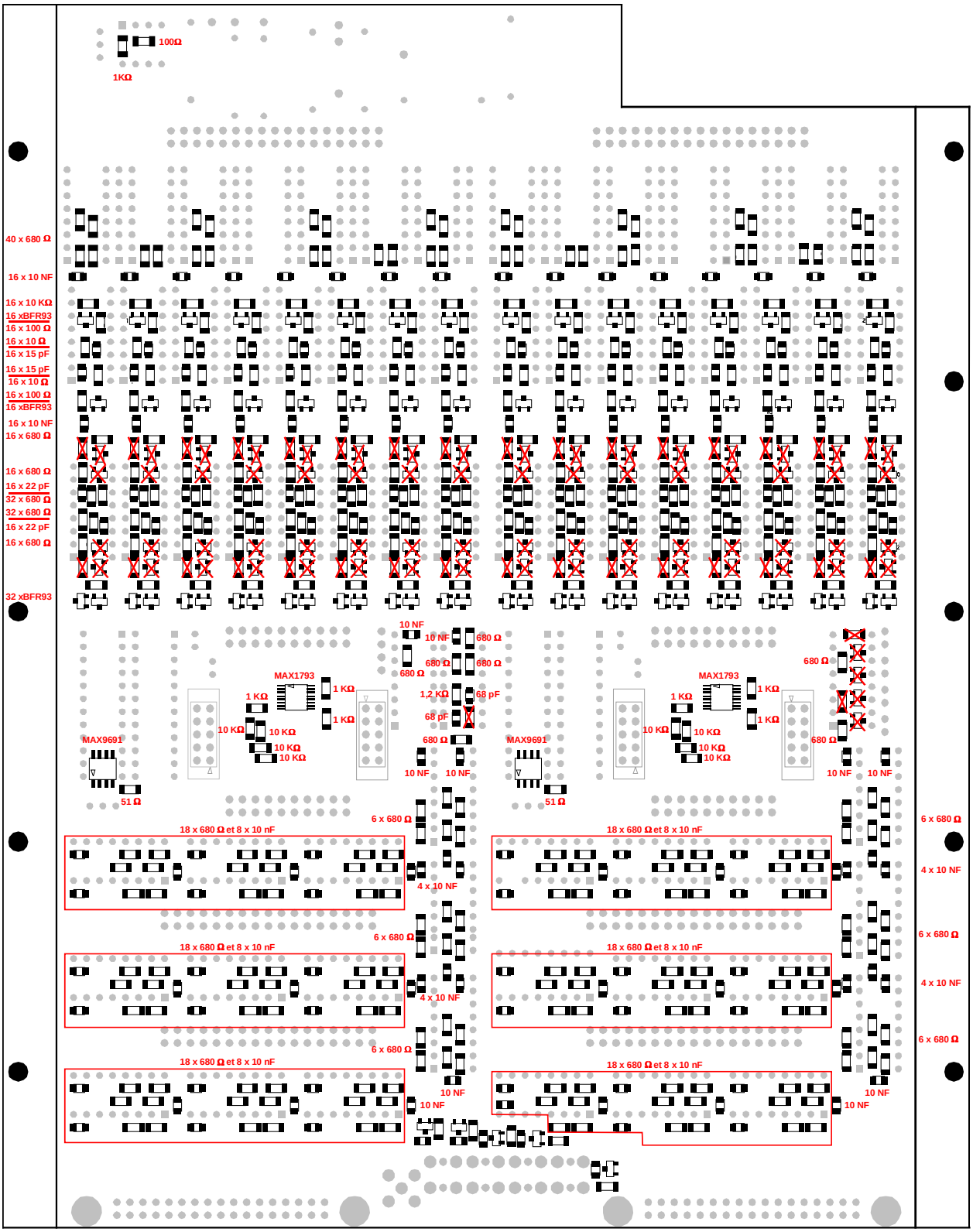


Annex 6 : component value (component board side)





Annex 7 : component value (sold side)



Annex 8 : bill of materials

Circuits logique :	
MC10H101_dip	17
MC10H109_dip	6
MC10H115_dip	8
MC10H124_dip	24
MC10H125_dip	1
MC10H131_dip	17
MC10H158_dip	1
MC10192_dip	1
SN10KHT5541_dip	4
EPM3256A-10 PQF144	2
MAX1793	2
MAX9691	2
NE5532_dip	1
OPA656_SO	2

Transistor & diodes :	
Transistor :	
BFR 93	106
Diode :	
30S6	1
UGB8BT	1

Résistances :	
10 (1206)	32
51 (1206)	3
100 (1206)	35
330 (1206)	2
680 (1206)	398
1 K(1206)	10
1,2 K(1206)	1
10 K(1206)	57
47 K(¼ W)	2

Reseau :	
100 (SIL8)	8

Potentiometre :	
10 K (10 tours)	4

Capacites :	
10 NF (0805)	148
15 pF (0805)	32
22 pF (0805)	32
68 pF (0805)	2
10 MF 25V	7
10 MF 25V droites	4

Connecteurs :	
HE10-2 male male	5
HE10-10 male male	4
HE10-20 male male	4
HE10_34 droit	6
HE10_34 coudes	2
HE10_34 à sertir	6
HE10_34 à sertir face avant)	6
Strap 2,54	7
LEMO coude simple	1
LEMO coude double	4

Annex 9 : MC10192 data sheet (ON semiconductor documentation)

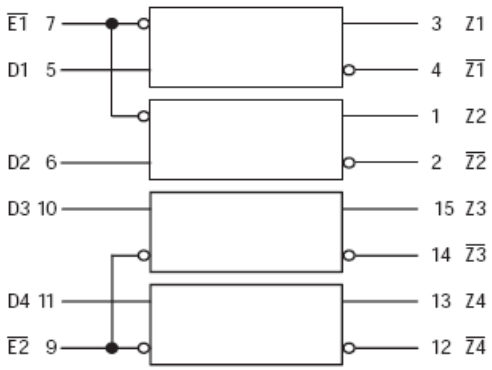
MC10192

Quad Bus Driver

The MC10192 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector. Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than –2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}. When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kW Input Pulldown Resistors on All Inputs (Unused Inputs May Be Left Open)
- Power Dissipation = 575 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ ($\overline{E}$ — Output)
  3.0 ns typ (D — Output)

LOGIC DIAGRAM



V_{CC} = PIN 16
V_{EE} = PIN 8

TRUTH TABLE

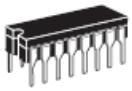
Inputs		Output	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

Note: Unused outputs must be terminated to V_{CC} for proper operation.

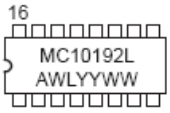
ON Semiconductor

http://onsemi.com

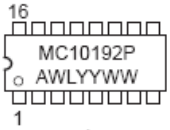
MARKING DIAGRAMS



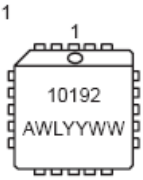
CDIP–16
L SUFFIX
CASE 620



PDIP–16
P SUFFIX
CASE 648

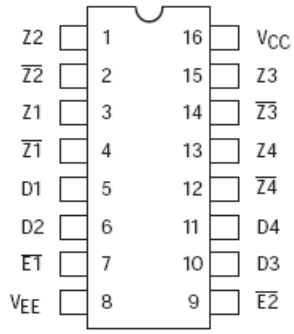


PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

ORDERING INFORMATION

Device	Package	Shipping
MC10192L	CDIP–16	25 Units / Rail
MC10192P	PDIP–16	25 Units / Rail
MC10192FN	PLCC–20	46 Units / Rail

March, 2000 – Rev. 6

Publication Order Number:
MC10192/D

Annex 10 : MC10H158 data sheet (ON semiconductor documentation)

MC10H158

Quad 2-Input Multiplexer

(Non–Inverting)

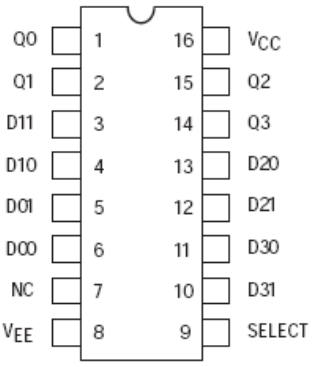
The MC10H158 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 197 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible

TRUTH TABLE

Select	D0	D1	Q
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

DIP PIN ASSIGNMENT

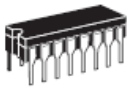


Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

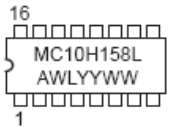
ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS

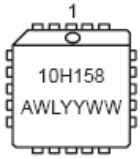


CDIP–16
L SUFFIX
CASE 620



PDIP–16
P SUFFIX
CASE 648

PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H158L	CDIP–16	25 Units/Rail
MC10H158P	PDIP–16	25 Units/Rail
MC10H158FN	PLCC–20	46 Units/Rail

Annex 11 : OPA656 data Sheet (Burr Brown documentation)

Burr-Brown Products from Texas Instruments

OPA656

SBOS196D – DECEMBER 2001 – REVISED AUGUST 2004

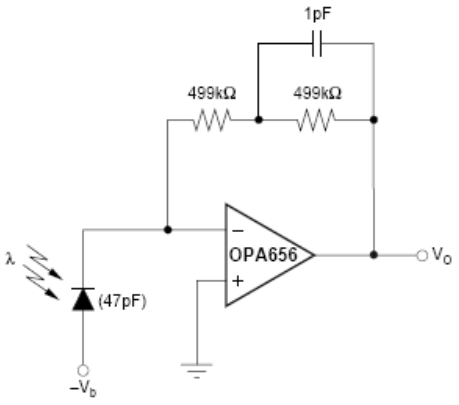
Wideband, Unity-Gain Stable, FET-Input OPERATIONAL AMPLIFIER

FEATURES

- 500MHz UNITY-GAIN BANDWIDTH
- LOW INPUT BIAS CURRENT: 2pA
- LOW OFFSET AND DRIFT: ±0.25mV, ±2µV/°C
- LOW DISTORTION: 74dB SFDR at 5MHz
- HIGH OUTPUT CURRENT: 70mA
- LOW INPUT VOLTAGE NOISE: 7nV/√Hz

APPLICATIONS

- WIDEBAND PHOTODIODE AMPLIFIERS
- SAMPLE-AND-HOLD BUFFERS
- CCD OUTPUT BUFFERS
- ADC INPUT BUFFERS
- WIDEBAND PRECISION AMPLIFIERS
- TEST AND MEASUREMENT FRONT ENDS



Wideband Photodiode Transimpedance Amplifier

DESCRIPTION

The OPA656 combines a very wideband, unity-gain stable, voltage-feedback op amp with a FET-input stage to offer an ultra high dynamic-range amplifier for ADC (Analog-to-Digital Converter) buffering and transimpedance applications. Extremely low DC errors give good precision in optical applications.

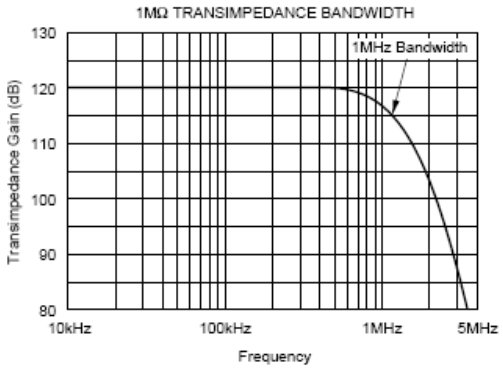
The high unity-gain stable bandwidth and JFET input allows exceptional performance in high-speed, low-noise integrators.

The high input impedance and low bias current provided by the FET input is supported by the ultra-low 7nV/√Hz input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

Broad transimpedance bandwidths are achievable given the OPA656's high 230MHz gain bandwidth product. As shown below, a –3dB bandwidth of 1MHz is provided even for a high 1MΩ transimpedance gain from a 47pF source capacitance.

RELATED OPERATIONAL AMPLIFIER PRODUCTS

DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/µS)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA355	+5	200	300	5.8	Unity-Gain Stable CMOS
OPA655	±5	400	290	6	Unity-Gain Stable FET-Input
OPA657	±5	1600	700	4.8	Gain of +7 Stable FET-Input
OPA627	±15	16	55	4.5	Unity-Gain Stable FET-Input
THS4601	±15	180	100	5.4	Unity-Gain Stable FET-Input



PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA, QUANTITY
OPA656U	SO-8 Surface Mount	D	–40°C to +85°C	OPA656U	OPA656U	Rails, 100
"	"	"	"	"	OPA656U/2K5	Tape and Reel, 2500
OPA656UB	SO-8 Surface Mount	D	–40°C to +85°C	OPA656UB	OPA656UB	Rails, 100
"	"	"	"	"	OPA656UB/2K5	Tape and Reel, 2500
OPA656N	SOT23-5	DBV	–40°C to +85°C	B56	OPA656N/250	Tape and Reel, 250
"	"	"	"	"	OPA656N/3K	Tape and Reel, 3000
OPA656NB	SOT23-5	DBV	–40°C to +85°C	B56	OPA656NB/250	Tape and Reel, 250
"	"	"	"	"	OPA656NB/3K	Tape and Reel, 3000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet. (2) UB and NB are high grade, while U and N are standard grade.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	$\pm V_S$
Input Voltage Range	$\pm V_S$
Storage Temperature Range	–40°C to +125°C
Lead Temperature	+260°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	200V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

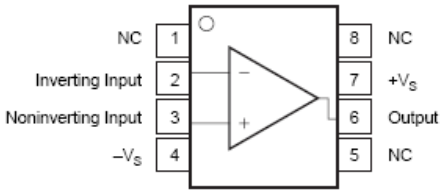
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

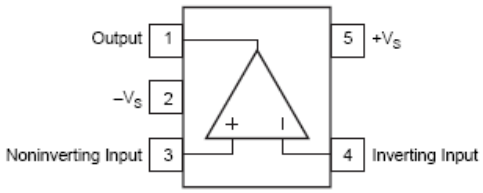
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

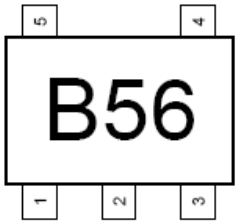
PIN CONFIGURATIONS

Top View SO



Top View SOT23





Pin Orientation/Package Marking

Annex 12 : Documentation update

Draft (July 2005) : initial version

Version 1 (August 2005) :

Annex : Generic pinout connector	Modify name
« SPLITTER & TRIGGER » board Diagram (Add MUX component MC10H158)	Modify
Add Annex 3 : Board scheme	Add
Add Annex 4 : board representation (component side)	Add
Add Annex 5 : board representation (sold side)	Add
Add Annex 6 : component value (component board side)	Add
Add Annex 7 : component value (sold side)	Add
Add Annex 8 : bill of materials	Add
Correct “Switches and setting” chapter (delay generator switch were wrong)	Modify
Add TABLE OF CONTENTS	Add
Add data sheet MC10192, MC10H158, OPA656 component	Add

Version 2 (September 2005) :

Board scheme up to date	Update

Version 3 (October 2005) :

Upgrade the “SPLITTER & TRIGGER board diagram” chapter 3	Update
In Inputµ/output chapter (chapter 2) add time duration of the MULTA MULTB signal	Add
In Inputµ/output chapter (chapter 2) add time duration of the TRIGGER0,TRIGGER1 signal	Add

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